Claims

[c1] What is claimed is:

1.A method of fabricating a metal-oxide semiconductor transistor (MOS transistor) on a substrate comprising:

sequentially forming a gate oxide layer and a gate on the substrate;

performing a first ion implantation process to form a first doped region in the substrate;

sequentially forming a dielectric layer and a sacrificial layer on the substrate;

forming a L-shaped spacer on either side of the gate;

performing a second ion implantation process to form a second doped region with a gradient profile in portions of the substrate adjacent to either side of the L-shaped spacer; and

performing a self-aligned silicide (salicide) process to form a silicide layer on the gate and on exposed portions of the substrate surface above the second doped region.

[c2] 2.The method of claim 1 wherein the substrate is a silicon substrate.

[c3] 3.The method of claim 1 wherein the gate comprises an offset spacer on either side of the gate.

[c4] 4.The method of claim 1 wherein a liner layer is formed to cover the substrate prior to the formation of the gate.

[c5] 5.The method of claim 4 wherein the L-shaped spacer is formed by the steps of:

performing a first etching process to simultaneously form an arc-shaped spacer on either side of the gate and remove portions of the dielectric layer and the sacrificial layer atop the gate;

performing a second etching process to remove portions of the sacrificial layer within the arc-shaped spacer; and

performing a third etching process to remove portions of the liner layer not covered by the L-shaped spacer.

[c6] 6.The method of claim 5 wherein the liner layer, the dielectric layer and the sacrificial layer respectively comprise silicon oxide, nitride and polysilicon.

[c7] 7.The method of claim 5 wherein the first etching process utilizes the liner layer as a stop layer, and the second etching process utilizes the dielectric layer as a stop layer.

[c8] 8.The method of claim 1 wherein the first and second doped regions are in a gradient profile, the first doped region is employed as a source/drain extension, and the second doped region comprises a step source/drain extension and a source/drain of the MOS transistor employed to prevent leakage current of the silicide layer.

[c9] 9.The method of claim 8 wherein the depth and the width of the step source/drain extension are respectively determined by the thickness of the dielectric layer and the width of the L-shaped spacer.

[c10] 10.The method of claim 8 wherein the silicide layer is formed by the steps of:
forming a metal layer on the gate and on portions of the substrate surface above the source/drain;
performing a first rapid thermal process (RTP);
performing a wet etching process to remove unreacted portions of the metal layer on the surface of the substrate; and
performing a second RTP.

[c11] 11.The method of claim 10 wherein the metal layer comprises cobalt (Co).

[c12] 12.The method of claim 1 wherein the first and second doped regions are doped with either arsenic (As) atoms or phosphorus (P) atoms.

[c13] 13.The method of claim 1 wherein the first and second doped regions are doped with either one of boron difluoride (BF_2^+) ions, boron (B) atoms or indium (In) atoms.

[c14] 14.A method of fabricating a MOS transistor on a substrate comprising:
sequentially forming a gate oxide layer and a gate on the substrate;
performing a first ion implantation process to form a first doped region in the substrate;
forming a liner layer to cover the substrate;

sequentially forming a dielectric layer and a sacrificial layer on the liner layer;
forming a L-shaped spacer on either side of the gate;
performing a first etching process to remove portions of the liner layer not covered by the L-shaped spacer;
performing a second ion implantation process to simultaneously form a second doped region and a third doped region in the substrate; and
performing a salicide process to form a silicide layer on the gate and on portions of the substrate surface above the third doped region.

[c15] 15.The method of claim 14 wherein the substrate is a silicon substrate.

[c16] 16.The method of claim 14 wherein the first, second and third doped regions are in a gradient profile and are respectively employed as a source/drain extension, a step source/drain extension and a source/drain of the MOS transistor, and the second doped region is employed to prevent leakage current of the silicide layer.

[c17] 17.The method of claim 14 wherein the liner layer, the dielectric layer and the sacrificial layer respectively comprise silicon oxide, nitride and polysilicon.

[c18] 18.The method of claim 14 wherein the L-shaped spacer is formed by the steps of:
performing a second etching process to form an arc-shaped spacer on either side of the gate and remove portions of the dielectric layer and the sacrificial layer atop the gate; and
performing a third etching process to remove portions of the sacrificial layer within the arc-shaped spacer.

[c19] 19.The method of claim 18 wherein the second etching process utilizes the liner layer as a stop layer, and the third etching process utilizes the dielectric layer as a stop layer.

[c20] 20.The method of claim 14 wherein the first, second and third doped regions are doped with either arsenic atoms or phosphorus atoms.

[c21] 21.The method of claim 14 wherein the first, second and third doped regions

are doped with either one of boron difluoride ions, boron atoms or indium atoms.

[c22] 22.The method of claim 14 wherein the depth and the width of the second doped region are respectively determined by the thickness of the dielectric layer and the width of the L-shaped spacer.

[c23] 23.The method of claim 14 wherein the silicide layer is formed by the steps of:
forming a metal layer on the gate and on portions of the substrate surface above the third doped region;
performing a first RTP;
performing a wet etching process to remove unreacted portions of the metal layer on the surface of the substrate; and
performing a second RTP.

[c24] 24.The method of claim 23 wherein the metal layer comprises cobalt.